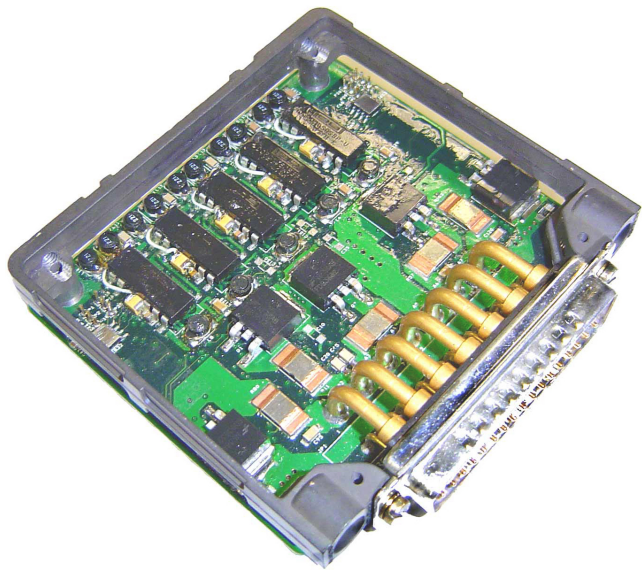


ENGINEERING DATA SHEET

EPM-109 SERIES

5-CHANNEL NEXT GENERATION SSPC
WITH TWO SSPCs UP TO 12A, DC RATING
PLUS THREE SSPCs UP TO 7.5A, DC RATING



DESCRIPTION

This LEACH Solid State Power Controller (SSPC) employs the latest micro-controller and Power FET technology incorporated into a Printed Circuit Board (PCB). The EPM-109 features non-derated switching for all types of load, while protecting against overload and short circuit. It features an extensive Built-In-Test (BIT) that verifies all critical functions at start-up and during operation. It is designed for operation in 28 VDC systems with a full rating of 3 channels of 7.5 Amps and 2 channels of 12 Amps.

SIZE: 91 x 91 x 23 mm

WEIGHT: 150 grams MAX.

FEATURES

- 3 channel rated at 7.5 Amps to 85°C
- 2 channel rated at 12 Amps to 85°C
- Power up and continuous BIT
- Serial data bus interface
- Programmable ratings (25%, 50%, and 75% of the rated value) and trip parameters
- Bounce free switching
- Fast acting
- Low voltage drop and power dissipation
- Software-based design for added configuration
- High voltage isolation
- No derating for lamp, motor and inductive loads

APPLICATION CHARACTERISTICS

- Serial control and monitoring capability
- Replaces electro-mechanical relay
- Continuous BIT
- Load status reporting
- Bounce free
- Long life, high reliability
- Trip on overloads
- Programmable ratings

Esterline Power Systems

Featuring **LEACH**® power and control solutions

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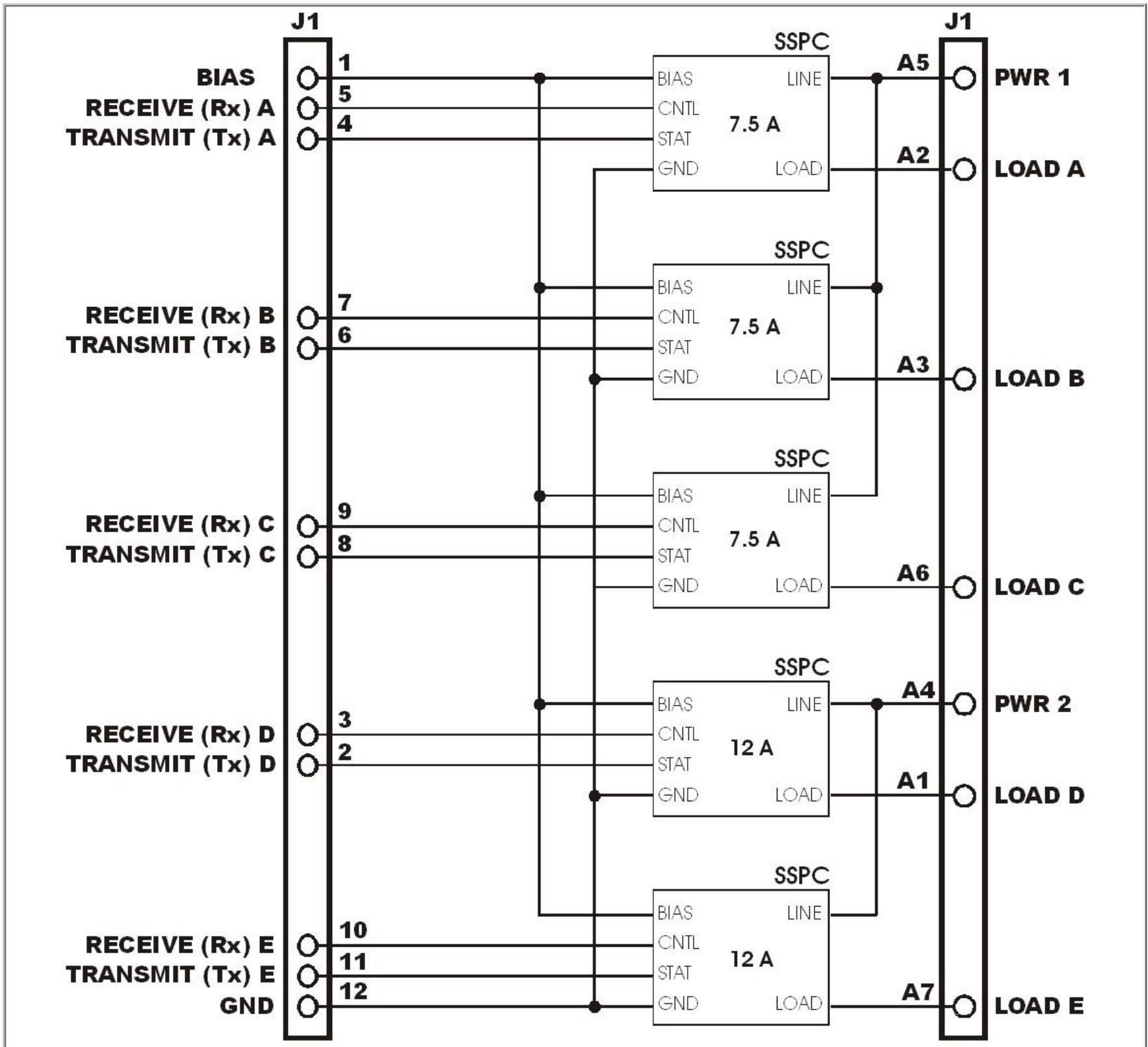
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Hong Kong

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Data sheets are for initial product selection and comparison. Contact Esterline Power Systems prior to choosing a component.



ENVIRONMENTAL DATA

Parameter	Symbol	Min.	Max.	Unit	Notes
Operational Temp. Range	T _{OP}	-40	+75	°C	1
Storage Temp. Range	T _{ST}	-55	+125	°C	1
Vibration		20 g, 20-2000 Hz			2
Acceleration		500 g			3
Shock		500 g, 0.5 ms			4
MTBF		100,000		hr/CH	

Notes: 1. See Thermal Derating Curve.

3. MIL-STD-883, Method 2001, Test Condition A.

2. MIL-STD-883, Method 2007, Test Condition A.

4. MIL-STD-883, Method 2002, Test Condition B.

ELECTRICAL CHARACTERISTICS

EPM-109 SERIES

Parameter	Symbol	Conditions	Limits		Unit	Notes
			Min.	Max.		
INPUT SPECIFICATIONS						
BIAS ON voltage	V_{ib}		4.5	5.5	V	(1,2)
BIAS ON current	I_{ib}		-	75	mA	(3)
RECEIVE voltage high	V_{ihr}		2.4	-	V	
RECEIVE voltage low	V_{ilir}		-	0.8	V	
RECEIVE current high	I_{ihr}	$V_{ihr} = 2.4 \text{ V}$	-	50	μA	
RECEIVE current low	I_{ilir}	$V_{ilir} = 0.4 \text{ V}$	-	-10	μA	
Transient voltage	V_t	Pulse width = 12.5 msec max. per DO-160D	-	+50	V	(4)
Spikes	V_s	Pulse width = 10 msec max. per DO-160D	-600	+600	V	(4)
OUTPUT SPECIFICATIONS						
Load Current	I_l		0	100	%rated I	(5)
ON state voltage drop	V_{ld}		-	200	mV	(6)
OFF state line voltage	V_l		-	70	V	(7)
Leakage current	I_{ll}		-	1	mA	(8)
Maximum let through current	I_{tr}		110	135	%rated I	
Dielectric withstanding voltage	V_{dw}		-	500	V_{RMS}	(9)
Insulation resistance	R_{ins}		100		M_{ohm}	(10)
TRANSMIT voltage high	V_{oht}	$I_{ot} = -4 \text{ mA}$	$V_{ib} * 0.8$		V	
TRANSMIT voltage low	V_{olt}	$I_{ot} = 4 \text{ mA}$		0.8	V	
TRANSMIT voltage rise time	T_{ort}	CL = 15 pf		3	ns	
TRANSMIT voltage fall time	T_{oft}	CL = 15 pf		3	ns	

Notes:

- (1) BIAS voltage must be a step function.
- (2) No reverse polarity protection.
- (3) BIAS voltage is +5.0Vdc.
- (4) The requirement apply only to the 28Vdc power line.
- (5) Load current is subject to thermal derating.
- (6) At load current $I_l = 100\%$ rated value.
- (7) Reverse polarity is not blocked and may damage the SSPC.
- (8) At $V_i = 28\text{Vdc}$, case temperature = 100°C .
- (9) 60 Hz, electrification time 10s, tested between each isolated section in turn groups (1,2 and 3), at sea level, ambient temperature, with the other two isolated sections shorted together.
- (10) 500Vdc, ± 10 .

TIMING

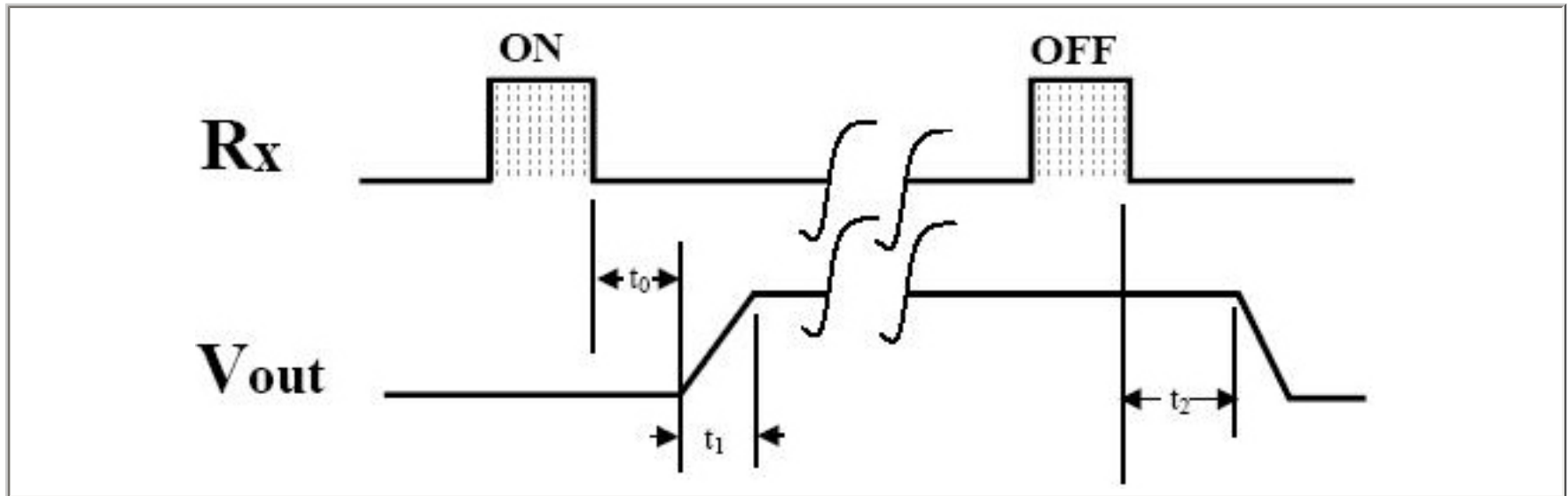
Parameter	SYMBOL	TYP	MAX.	UNITS	NOTE
RECEIVE to ON delay	t_0	500	2000	μsec	
Output voltage rise time	t_1	50	500	μsec	1
RECEIVE to OFF delay	t_2	500	2000	μsec	2

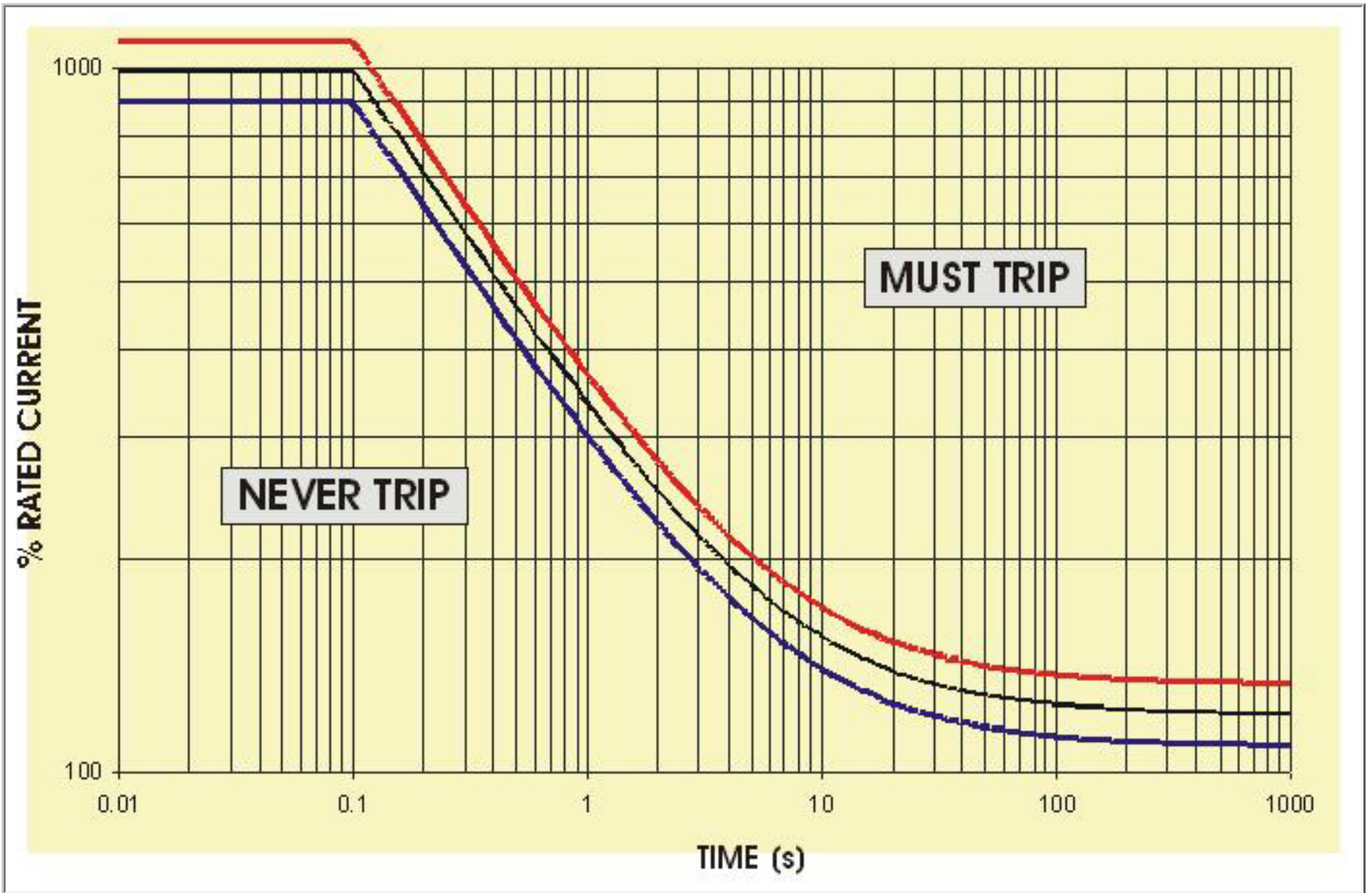
Notes:

(1) Timing measurements taken at 10% and 90% points into resistive rated load.

(2) Delay time from trip dependant on overload condition.

TIMING DIAGRAM





THERMAL DERATING

